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TWO BIT ERROR DETECTION AND CORRECTION IN SRAM-BASED EMULATED TCAMs

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ABSTRACT

In recent years, numerous methods have been introduced to emulate TCAMs on FPGAs. Some of these approaches leverage the abundant memory blocks accessible within modern FPGAs to create TCAM-like functionality. One notable challenge when employing memory based solutions is their susceptibility to soft errors that can corrupt stored data. This project presents a novel approach for addressing double-bit errors in SRAM-based emulated Ternary Content Addressable Memories (TCAMs). TCAMs are essential for high-speed search operations in networking and data storage systems but are prone to soft errors, particularly in SRAM-based emulations. To enhance error resilience, we propose the use of the DBEC Algorithm for detecting and correcting the first Bit error, and a using Single Error Correction (SEC) decoder for addressing the second error. The DBEG Algorithm detects and fixes one errors, minimizing performance overhead, while the SEC decoder provides an additional layer of protection, correcting any remaining errors. This dual-error correction strategy ensures robust error handling with minimal impact on latency and resource utilization. Results demonstrate that the proposed solution improves the reliability of SRAM-based TCAMs under heavy error conditions, making them suitable for critical applications in networking and high-speed data processing environments.

INTRODUCTION

In modern computing and networking applications, Ternary Content Addressable Memory (TCAM) is widely used for high-speed search operations, such as IP address lookup, packet classification, and security filtering. However, conventional TCAMs suffer from high power consumption and limited scalability, leading to the development of SRAM-based emulated TCAMs as an efficient alternative. These emulated TCAMs leverage traditional SRAM arrays along with logic-based architectures to achieve TCAM functionality while reducing power consumption and improving flexibility.

Despite these advantages, SRAM-based emulated TCAMs remain susceptible to soft errors caused by radiation-induced bit flips, affecting the reliability of data storage and retrieval. Single-bit error detection and correction techniques have been commonly employed to mitigate such errors. However, as memory systems become more complex and data integrity requirements increase, single-bit error correction is insufficient in many scenarios. Therefore, robust two-bit error detection and correction (EDAC) mechanisms are essential for enhancing the reliability of SRAM-based TCAM architectures.

This research focuses on developing an efficient two-bit error detection and correction scheme for SRAM-based emulated TCAMs. By integrating error correction codes (ECC) and optimized fault-tolerant architectures, the proposed approach aims to improve data integrity, minimize error propagation, and ensure high-speed memory operations without significant performance overhead.

LITERATURE SURVEY

- "Peng He, Wenyuan Zhang, Hongtao Guan, Kavé Salamatian, and Gaogang Xie (IEEE/ACM Transactions on Networking, 2018)" analyze TCAMs for rapid packet matching but highlight their high update costs. The study applies partial order theory to optimize rule ordering in TCAMs, identifying optimal update algorithms and performance limits. A heuristic based on ruleset partitioning reduces update costs by 1.05 to 11.3 times compared to existing methods.

- "Alexis Ramos, Ricardo G. Toral, Pedro Reviriego, and Juan Antonio Maestro (IEEE Transactions on Computers, 2018)" propose a strategy to protect soft processors in SRAM- based FPGAs from cosmic radiation. The approach uses a library of adaptive protection configurations based on application profiling and FPGA reconfiguration capabilities.

- "S. Lokesh and S. Sadiq Basha (Sathyabama Institute of Science and Technology, 2021)" address the vulnerability of SRAM-based TCAMs to soft errors in SDN [2] and OpenFlow applications. The paper proposes error detection and correction techniques for SRAM- based TCAMs of various sizes, demonstrating improvements in area, delay, and power performance through Verilog HDL designs and Xilinx Vertex 5 FPGA synthesis.

- "T.L. Spandana and J.S. Rose Victor (Amrita Sai Institute of Science & Tech, IJETT, 2013)" present a multi-pattern matching algorithm using TCAM for efficient pattern decoding and database storage. They propose an adaptive dual-port BiTCAM for high- speed, low-power, and low-cost pattern detection, reducing transistor count and power consumption compared to single-port schemes and offering flexibility for virus database updates.

PROPOSED SYSTEM

Single bit error detection and correction in SRAM-BASED TCAM

To calculate the parity bits, the Hamming code uses a set of equations that combine the bits in the code word. These equations are based on the binary representation of the Hamming distance between the code word and all possible data words. The Hamming distance is the number of bits that differ between two words of the same length.

For 4-bit data bits the needed parity bits are, P1 = D1 XOR D2 XOR D4

P2 = D1 XOR D3 XOR D4

P3 = D2 XOR D3 XOR D4

First, we need to determine the positions of the parity bits in the code word. In this case, we can use the following parity bit positions:

Bit [7]: D1

Bit [6]: D2

Bit [5]: D3

Bit [4]: P3

Bit [3]: D4

Bit [2]: P2

Bit [1]: P1

Single error detection and correction

Single bit error detection can be used with the help of parity bits and correction can be done with the help of SEC decoder.

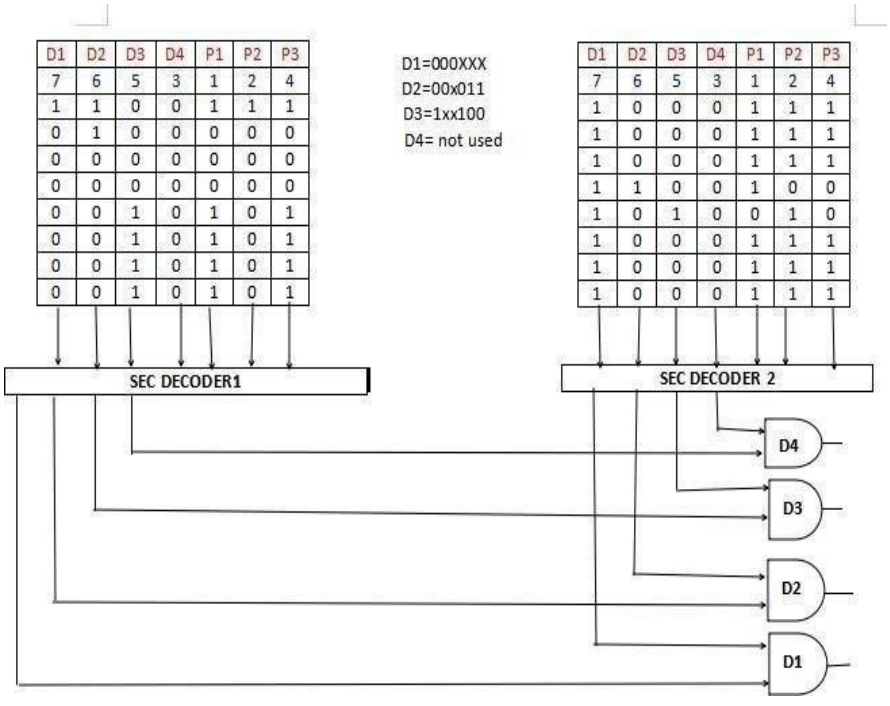

Figure.1 Single bit error detection and correction

Double bit error detection and correction using DBEC Algorithm

Currently, various techniques exist for detecting and correcting single-bit errors in SRAM- emulated TCAMs. We introduce a new method called the DBEC (Double Bit Error Correction) algorithm. Extended Parity Bit is used along with the data bits and parity bits to detect the double bit error in the SRAM based TCAMS For correction , DBEC(Double Bit Error Correction) algorithm corrects the single bit error and the remaining second error is corrected using the SEC decoder. Block diagram of Two-bit error detection and correction is given below.

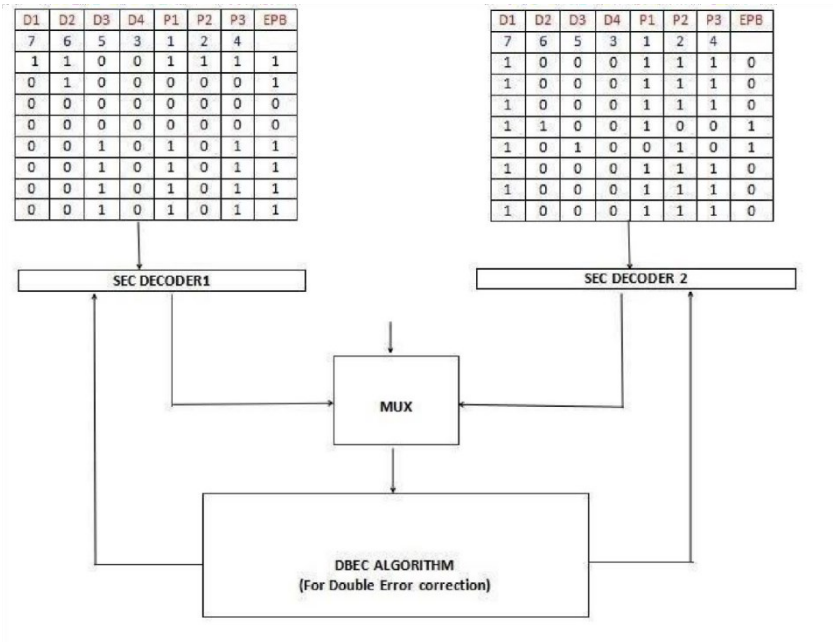

Figure.2 Double bit error detection and correction process

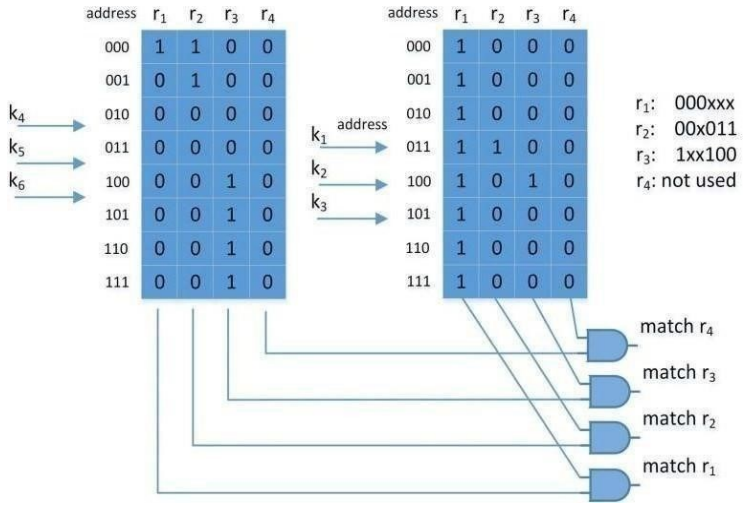

Figure.3 SRAMs and Matching circuit the DBEC

STIMULATION RESULTS

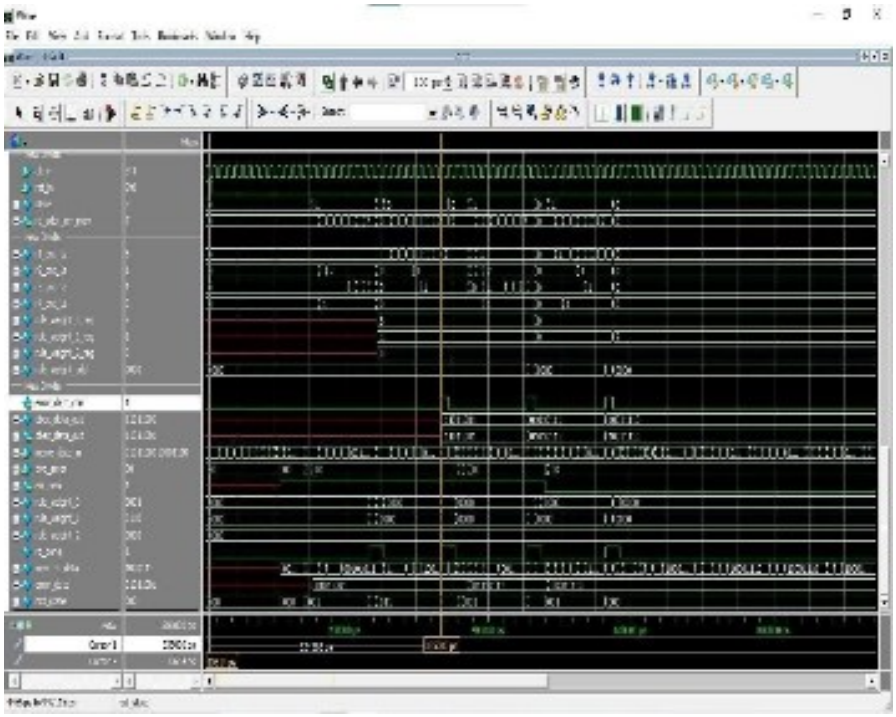

Figure.4 Single bit error detected and corrected

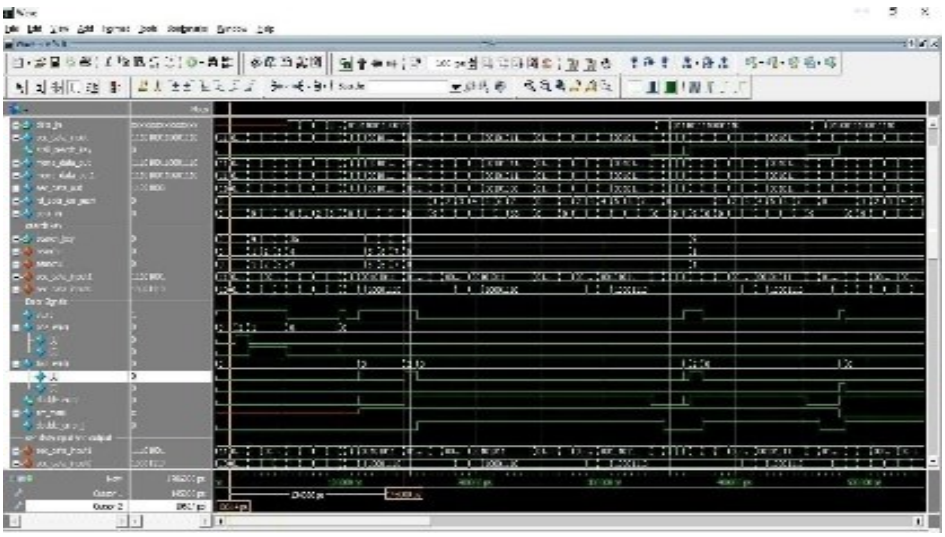

Figure.5 Two-Bit error Detection

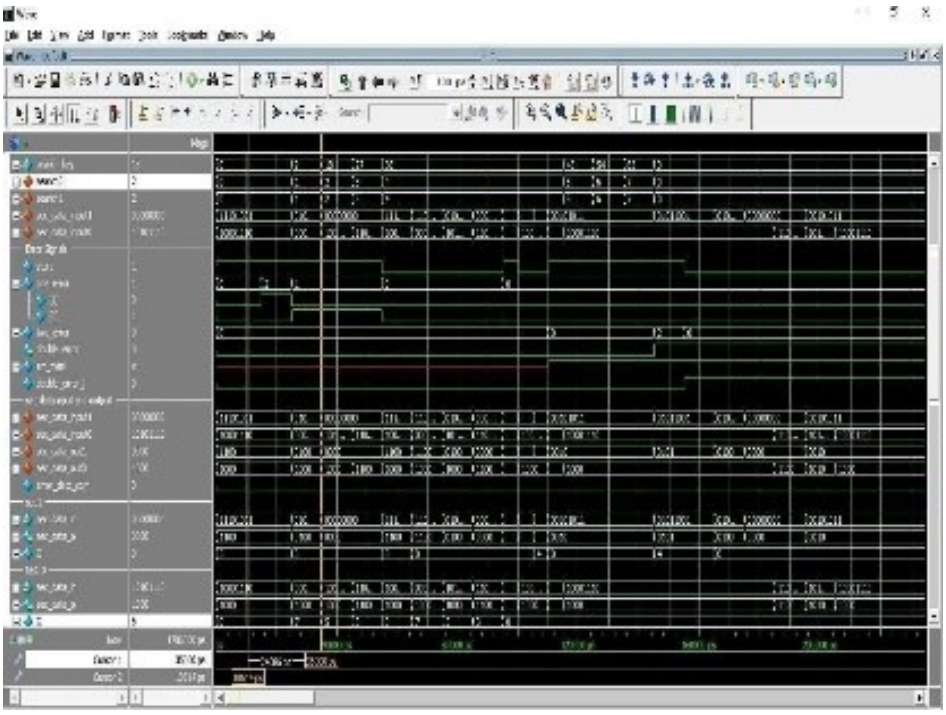

Figure.6 TWO -bit error 1st bit Detected using DBEC algorithm

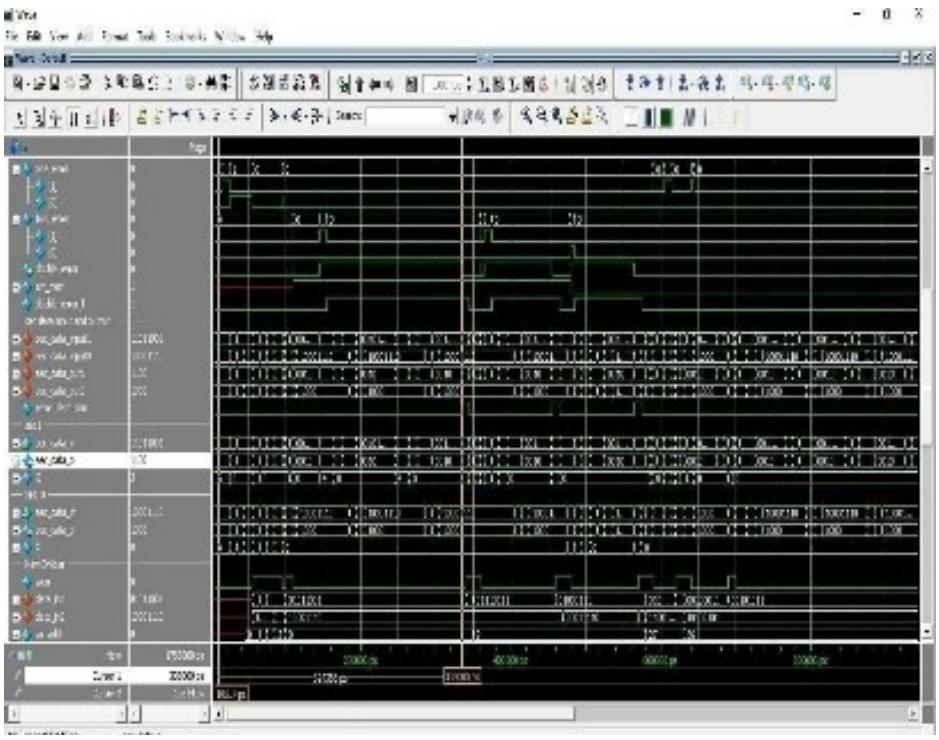

Figure.7 TWO- bit error 2nd bit Detected using SEC decoder

ADVANTAGES

Enhanced Reliability: By detecting and correcting errors brought on by a variety of circumstances, such as power fluctuations, radiation, or manufacturing flaws, error detection and correction can be implemented in SRAM emulated TCAMs to increase the system's reliability.

Minimized Downtime: By detecting and correcting errors in real time, system downtime brought on by malfunctioning TCAMs can be greatly decreased, increasing overall system availability.

Better Performance: By stopping performance deterioration in TCAMs, error detection and correction systems may guarantee ideal system performance.

Cost-Effectiveness: By extending the life of malfunctioning TCAMs, error detection and correction procedures can lower the requirement for frequent replacements and save money.

Enhanced Security: Error detection and correction techniques can improve the security of TCAM-stored data, guaranteeing data integrity, in network applications like firewalls and intrusion detection systems.

APPLICATIONS

TCAMs are frequently found in routers, switches, and firewalls in networking to provide quick packet forwarding, filtering, and classification. Error detection and Correction can be added to TCAMs to increase these networking devices' accessibility and dependability.

- TCAMs are also utilized by the telecommunications industry in call routing and switching gateways, radio network controllers, and base stations. TCAMs that incorporate error detection and correction can assist avoid mistakes that could lead to missed calls or poor communication.
- TCAMs are essential to data centres for tasks including traffic control, load balancing, and security. The trustworthy and effective operation of these applications may be guaranteed by error detection and correction in TCAMs.
- TCAMs are crucial for operations including target tracking, image processing, and radar signal processing in the aerospace and defence industries. These crucial functions can be made more accurate and reliable by including error detection and correction into TCAMs.

CONCLUSION

In conclusion, the evolution of TCAM emulation on FPGAs has seen significant advancements, particularly in leveraging FPGA memory blocks for TCAM-like functionalities. However, the susceptibility of memory-based solutions to soft errors remains a critical challenge. Addressing this challenge, this investigation focuses on enhancing the security and resilience of these memory systems.

A novel approach has been demonstrated with the implementation of a 2-bit Error Detection and Correction mechanism, integrating a Single Error Correction (SEC) decoder and a specialized debugging algorithm. This

dual-layer strategy represents a pioneering step towards fortifying the reliability and robustness of TCAM emulation techniques, marking a significant advancement in the field.

FUTURE SCOPE

Addressing double bit errors in TCAMS " is a field of research that deals with improving the reliability of ternary content-addressable memories (TCAMs) using error detection and correction techniques. TCAMs are widely used in network routers, firewalls, and other high- speed network devices for packet classification and routing.

Developing more efficient error detection and correction techniques: Researchers can explore new methods to detect and correct errors in SRAM emulated TCAMs that are more efficient than existing techniques. These techniques can reduce the overhead and improve the accuracy of error detection and correction.

Designing fault-tolerant SRAM emulated TCAM architectures: Researchers can focus on developing new architectures that are more fault-tolerant and can withstand more errors without compromising the accuracy of packet classification.

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