TWO BIT ERROR DETECTION AND CORRECTION IN SRAM-BASED EMULATED TCAMs

Mrs.D.V.V.LAKSHMI $^1\!,$ A.GAYATHRI PUSHPA $^2\;$, D.LOKESH 3 , K.L.T.ANVITHA SRI $^4\;$, G.DAKSHAYANI 5 , M.A.YATIN SHARMA $^6\;$

¹Assistant Professor, Dept. Of ECE, PRAGATI ENGINEERING COLLEGE

²³⁴⁵⁶UG Students, Dept. Of ECE, PRAGATI ENGINEERING COLLEGE

ABSTRACT

In recent years, numerous methods have been introduced to emulate TCAMs on FPGAs. Some of these approaches leverage the abundant memory blocks accessible within modern FPGAs to create TCAM-like functionality. One notable challenge when employing memory based solutions is their susceptibility to soft errors that can corrupt stored data. This project presents a novel approach for addressing double-bit errors in SRAM-based emulated Ternary Content Addressable Memories (TCAMs). TCAMs are essential for high-speed search operations in networking and data storage systems but are prone to soft errors, particularly in SRAM-based emulations. To enhance error resilience, we propose the use of the DBEC Algorithm for detecting and correcting the first Bit error, and a using Single Error Correction (SEC) decoder for addressing the second error. The DBEG Algorithm detects and fixes one errors, minimizing performance overhead, while the SEC decoder provides an additional layer of protection, correcting any remaining errors. This dual-error correction strategy ensures robust error handling with minimal impact on latency and resource utilization. Results demonstrate that the proposed solution improves the reliability of SRAM-based TCAMs under heavy error conditions, making them suitable for critical applications in networking and high-speed data processing environments.

INTRODUCTION

In modern computing and networking applications, Ternary Content Addressable Memory (TCAM) is widely used for high-speed search operations, such as IP address lookup, packet classification, and security filtering. However, conventional TCAMs suffer from high power consumption and limited scalability, leading to the development of SRAM-based emulated TCAMs as an efficient alternative. These emulated TCAMs leverage traditional SRAM arrays along with logic-based architectures to achieve TCAM functionality while reducing power consumption and improving flexibility.

Despite these advantages, SRAM-based emulated TCAMs remain susceptible to soft errors caused by radiationinduced bit flips, affecting the reliability of data storage and retrieval. Single-bit error detection and correction techniques have been commonly employed to mitigate such errors. However, as memory systems become more complex and data integrity requirements increase, single-bit error correction is insufficient in many scenarios. Therefore, robust two-bit error detection and correction (EDAC) mechanisms are essential for enhancing the reliability of SRAM-based TCAM architectures.

This research focuses on developing an efficient two-bit error detection and correction scheme for SRAM-based emulated TCAMs. By integrating error correction codes (ECC) and optimized fault-tolerant architectures, the proposed approach aims to improve data integrity, minimize error propagation, and ensure high-speed memory operations without significant performance overhead.

LITERATURE SURVEY

- "Peng He, Wenyuan Zhang, Hongtao Guan, Kavé Salamatian, and Gaogang Xie (IEEE/ACM Transactions on Networking, 2018)" analyze TCAMs for rapid packet matching but highlight their high update costs. The study applies partial order theory to optimize rule ordering in TCAMs, identifying optimal update algorithms and performance limits. A heuristic based on ruleset partitioning reduces update costs by 1.05 to 11.3 times compared to existing methods.
- "Alexis Ramos, Ricardo G. Toral, Pedro Reviriego, and Juan Antonio Maestro (IEEE Transactions on Computers, 2018)" propose a strategy to protect soft processors in SRAM- based FPGAs from cosmic radiation. The approach uses a library of adaptive protection configurations based on application profiling and FPGA reconfiguration capabilities.
- "S. Lokesh and S. Sadiq Basha (Sathyabama Institute of Science and Technology, 2021)" address the vulnerability of SRAM-based TCAMs to soft errors in SDN [2] and OpenFlow applications. The paper proposes error detection and correction techniques for SRAM- based TCAMs of various sizes, demonstrating improvements in area, delay, and power performance through Verilog HDL designs and Xilinx Vertex 5 FPGA synthesis.
- "T.L. Spandana and J.S. Rose Victor (Amrita Sai Institute of Science & Tech, IJETT, 2013)" present a multipattern matching algorithm using TCAM for efficient pattern decoding and database storage. They propose an adaptive dual-port BiTCAM for high- speed, low-power, and low-cost pattern detection, reducing transistor count and power consumption compared to single-port schemes and offering flexibility for virus database updates.

PROPOSED SYSTEM

Single bit error detection and correction in SRAM-BASED TCAM

To calculate the parity bits, the Hamming code uses a set of equations that combine the bits in the code word. These equations are based on the binary representation of the Hamming distance between the code word and all possible data words. The Hamming distance is the number of bits that differ between two words of the same length.

For 4-bit data bits the needed parity bits are, P1 = D1 XOR D2 XOR D4

$$P2 = D1 XOR D3 XOR D4$$

P3 = D2 XOR D3 XOR D4

First, we need to determine the positions of the parity bits in the code word. In this case, we can use the following parity bit positions:

Bit [7]: D1

Bit [6]: D2

Bit [5]: D3

Bit [4]: P3

Bit [3]: D4

Bit [2]: P2

Bit [1]: P1

Single error detection and correction

Single bit error detection can be used with the help of parity bits and correction can be done with the help of SEC decoder.



Figure.1 Single bit error detection and correction

Double bit error detection and correction using DBEC Algorithm

Currently, various techniques exist for detecting and correcting single-bit errors in SRAM- emulated TCAMs. We introduce a new method called the DBEC (Double Bit Error Correction) algorithm. Extended Parity Bit is used along with the data bits and parity bits to detect the double bit error in the SRAM based TCAMS For correction, DBEC(Double Bit Error Correction) algorithm corrects the single bit error and the remaining second error is corrected using the SEC decoder. Block diagram of Two-bit error detection and correction is given below.



Figure.2 Double bit error detection and correction process



Figure.3 SRAMs and Matching circuit the DBEC

STIMULATION RESULTS

e (98		and the second second					- 77		-				-	-
30.91	485210-	HE 93	西蒙市	-	84 R	12 pr	112	125	12 23	tatia-	福泉 月	·9.98	·4	
월 신 L # 13	1	11.35					4.54	HAR	1.363		1.1			
	at here the second second			1.000		-	8.24		12.00.1		1.1.5			
4.14	Ho			_				_						_
alt.		incon:	nerrer	more	miner	hhh	12222	heer	111111111	000000000000000000000000000000000000000	in man	contranc	or the second	1111
10		f				1								-
1.00				1000	111		1: 5		34	1:				
optimizer .		1		1000			() and ()	din i	3120000					
1.8.4						1200								
00				11.		٩			2 1	10				
		₩		- Li			- 21		- <u>1</u>					-
itata Alexandre				-	-				~ "	_6				
Legila									÷	10	_			-
stungtung -					1									
a la anna a la anna anna anna anna anna		100					- C		300	1100				
a 246		1												
AND A COMP.	1						1		1	л				
da, dia su	121.20						R (B)		0.0044	(ROTAL)				
der, den jan		1000			-		101.15		Jonn's State	INCOME.				
ACR DC R		μ mm				р.		.uu=					00_0101	10 <u>-</u>
2012		1		18			1100		1.4					
nten State	xi			_	11100		100		711102	(1920)	_		_	_
NUMPU		L.	_		1100		100		1 Jon	1123				
A suffi	201	÷		_	14/25									-
-UNI		1								m				
an i dia	NCT		- K -	110100	and the state	120	12030	124		1011110	100111-1	TODUCT	(Instant)	11000
ars:				10/107			OFF	1	HEAD					
TT JONE	×	12	- 10	KI	in.		Der		: ku	1x				
	36.5	1.00							1 1 1 1					
Quer.	all and a second se			10.00	•		41 (y)			Mark pr			81.	
110				18.4		1.1								



	12258(15	BS210-	At e	2.328 Steel	2 xx + 44 20	Sec: 28	191.4	1. 5-9-9	5.6
Arrow Construction Arrow C	1 1 N C 2 F								
Arrow Construction Arrow C	6- C.	14.5			in the second se				
Answer Answer<	ed staja						in the second	her's	i promition the
Security is a state of the state o	A REALING		CINE OF						
Add 1 Second	Section 2.								
Markan Source Source<	in the state of the		112 101		- Contract from the	20. 1 I I I I	ALC: HILL:	THE REPORT	
Adda system Control Sector Control Sector </td <td></td> <td></td> <td>0.00</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>			0.00						
Second Instance Second Ins	NUMBER OF		0.000			(a) 1 (1) 1 (b)	aa 111000	L D D D XXX	
and in and in and in and in and in and in bit in the interval of	tang ng pangla 🚰		C			1 1 1 1 1 1 1 1 1 1	and the second second	CONTRACTOR OF	
State Control Control <thcontrol< th=""> <thcontrol< th=""> <thcon< td=""><td></td><td></td><td>G</td><td></td><td>3:101102</td><td>2 50111</td><td>1 3 5133</td><td></td><td>3 231111</td></thcon<></thcontrol<></thcontrol<>			G		3:101102	2 50111	1 3 5133		3 231111
Second Description Second	id and by						X		
Society of the second state Society of the secon	S and a second sec		0.000	2014 (s.2015)					
	A MARTI		(1) (1) (1)	22514 (826) (826) (826)			1		
Introduct Social Social <	Manjah Jadi								
	w so inte		128.11	C 1 1 1 C 1 C 1 Contact	 1 () (2000120) 	1:1:	000000	1.1.1.222122	
A model									
Image: part of a state of the state of t					1				F
Validation Validation Validation <td>1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</td> <td></td> <td>12 212</td> <td>14 2</td> <td></td> <td></td> <td></td> <td></td> <td></td>	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		12 212	14 2					
Validation Validation Validation <td>1. 2</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>_</td> <td></td>	1. 2							_	
Villen: Villen:	and the second		-						
Villen: Villen: Villen:				12 2	12			•	12
A following Image: Control of Contro									r
<pre>Si Press Si Mary 1 - 200. PL - Control - Si Divert - Control - Cont</pre>									
Ability or and a second sec		80 C							
e bengangan and Magangan and Magangangan Magangan and Magangan Magangangan Magangangan Magangangan Magangangan Magangangan Magangangan Magangangangan Magangangan Magangangangan Magangangan Magangangangan Magangangangan Magangangangan Magangangangangangan Magangangangangan Magangangangangangangangan Magangangangangangangangan Magangangangangangangangan Magangangangangangangangan Magangangangangangangangan Magangangangangangangangan Magangangangangangangangan Magangangangangan Magangangangangan Magangangangangangan Magangangangangan Magangan		20 C							
Bit Control All Description Control Contro Control <thcontrol< th=""></thcontrol<>									
According Differ Differ <thdifer< th=""> <thdifer< th=""> Difer<td></td><td></td><td></td><td>The second s</td><td>And Designed</td><td>21. 1 11. Inc.</td><td>NY 1 1101 1</td><td>A Disc Descents</td><td>The second second</td></thdifer<></thdifer<>				The second s	And Designed	21. 1 11. Inc.	NY 1 1101 1	A Disc Descents	The second second
eli ten illición o contra della por trata entre ordena della porte della port			0.00	11.000.02		1 1	10011	1 1 2 2 2 1 2	
0 000 2 180 p 11 18 7 40 p 10 18 7 40 p 10 18 7 40 p				CONTRACTOR OF THE OWNER OWNER OF THE OWNER	In the local division of the local divisiono		****		
0.00 2 (R:/p) 00+p			¥			TC-017		400 pc	20106.06
	the second s			D600 p	3				
	0.00 2								

Figure.5 Two-Bit error Detection

- 212 222351312	0.5310-4	42 F.F	-68	51	ne y	metald	古里	· 11일0	1 + + + 1 ±-	송: 미·명·	84.4
	上日H++	1.1 3		- Jarc		120.5	4	a a b d a	TIM	1.12	
	Higi										
d nit la			1;		X			14 191	20 0		
) 🌵 Manti	2	3000	1;	1	1.			1: 15	() () ()		
and the second se		1000	11	2 2 2	1.			16 16	10 D		
Nu stead		00250				- XB. (CX		2.68	0.325	3.9" (2008)	
w wateralt		1000.16	122	21.10	1206 1202	in or i	- 	1200122		100	Line finance
Dan Ayrık							_				
121		5 14	1				. —				
Los T		<u> </u>	-				-				
1 ST											
Mark and		2						5	12 30		
Linker.		-									
diana di second							-				
 deltagent j 										-	
-sectors and a coded											
and the second se	200000	108.0		00,000		- XB. 40X - 1			12031005	And Comment	10000
		1007-16		2 a 100		- H - H - H	- C.	100110			- JAP TOXIC
	205	100	12.0			1000 (1000 - 1		2.2	0.0	200 (000	ixa
		300	0.001	20, 100	1000 1000	inter (conti-	2	1200		100	ing the
a mutator	19 A										
A water	a ann	Import	Cit.	1000000	bur the	. len. 100. 1	17	XXX R.1	location.	log. Compte	tagen
		(100	1.101		1100 111		÷	Day.	1201	300 100	120
4		1	r	-	1 10		_	-0	14	Y	
-16: 1											
d work?		1000.100	0.8	12 . 118.	158. 181	IN US 1	122	1200125		1000	. IKL LORIC
N NORD		100	1.01	0 (00	Taun 1.14	1000011000	1.15	1.00			a factor for the second second
141	5	Contract of the local division of the local	17		12 17	1.000					
a lor	(1873) pt.	1 1 1 F 1	1	NUMER OF		ston sc			540		23.00 (

Figure.6 TWO -bit error 1st bit Detected using DBEC algorithm

-2253 14	8.0.1 0 MF	SUERI	919 ma	M	LELE	6111319	10112-	at 1.4.4	13. II
34 TELL	22H4326	1 3.4.7	Sauce	*	84.6 4	44.523		1.3 1	
	hipi								
374 (418)	1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1	2 3					Satis t		
124				-					
A to see		3 1			10.0	.to			
14.1		i i i i i i i i i i i i i i i i i i i							
182.						1			
Sale est					1				
Politicer									
A taken and and	20				4-4	-			
A record and		101200-1	1001	122 101	1011 10		10 10 10 10 10 10 10 10 10 10 10 10 10 1	- 1331 38 - 13	0.00-10-135
a maria a spatta	autre de la companya	1 111 1 2 2 2001	and fuero		115	CI 111 10			C LOOLIN C LLC
A MORECUS		1011 10m. 1	111100	1110.00	101011-020		AND DEDUCTION	100 br. 11	1 Dec. 101 Dec
Lander C		NAME OF BRIDE	0.000	10.22		c nebe		222 (; 1020	1100 110
Sew incom	12								
aci	1995								
Maria Maria	And a local division of the local division o	1014200.	KZL.		HEAD POINTS			- 1010 - M 11 - 1010 - M 11	
Call (1000	1 10 14			101012 12	13			AC .11 182
	1			ſ"	and a second				
S MONT	2011.2	COULD STORE	C.10.11	11728	· 065	RE 1020	D. CHARLES	as of thisses	CONSISTER OF STREET
ويقويه الأ	20 1 1	NINDER COMME	0.000	10.02				322 0 2 1000	100000000000000000000000000000000000000
19:	100	10018				111.2	1.50		
Herbiter	62.							-	
Al esta Table a fac	1100	TTT INCOME			-	- Landard		DE CRET	
A dat 10	200142	OT DELET			100000	District in	11:10 - 10		
Standi		8 (12)3				L'AND &	12 18		
11 tr	15000.0				40,001.02	100		1.1.1.2.2	
5 m i	Z000 ::		2000js No	100			00000 pr		10060 pr

Figure.7 TWO- bit error 2nd bit Detected using SEC decoder

ADVANTAGES

Enhanced Reliability: By detecting and correcting errors brought on by a variety of circumstances, such as power fluctuations, radiation, or manufacturing flaws, error detection and correction can be implemented in SRAM emulated TCAMs to increase the system's reliability.

Minimized Downtime: By detecting and correcting errors in real time, system downtime brought on by malfunctioning TCAMs can be greatly decreased, increasing overall system availability.

Better Performance: By stopping performance deterioration in TCAMs, error detection and correction systems may guarantee ideal system performance.

Cost-Effectiveness: By extending the life of malfunctioning TCAMs, error detection and correction procedures can lower the requirement for frequent replacements and save money.

Enhanced Security: Error detection and correction techniques can improve the security of TCAM-stored data, guaranteeing data integrity, in network applications like firewalls and intrusion detection systems.

APPLICATIONS

TCAMs are frequently found in routers, switches, and firewalls in networking to provide quick packet forwarding, filtering, and classification. Error detection and Correction can be added to TCAMs to increase these networking devices' accessibility and dependability.

- TCAMs are also utilized by the telecommunications industry in call routing and switching gateways, radio network controllers, and base stations. TCAMs that incorporate error detection and correction can assist avoid mistakes that could lead to missed calls or poor communication.
- TCAMs are essential to data centres for tasks including traffic control, load balancing, and security. The trustworthy and effective operation of these applications may be guaranteed by error detection and correction in TCAMs.
- TCAMs are crucial for operations including target tracking, image processing, and radar signal processing in the aerospace and defence industries. These crucial functions can be made more accurate and reliable by including error detection and correction into TCAMs.

CONCLUSION

In conclusion, the evolution of TCAM emulation on FPGAs has seen significant advancements, particularly in leveraging FPGA memory blocks for TCAM-like functionalities. However, the susceptibility of memory-based solutions to soft errors remains a critical challenge. Addressing this challenge, this investigation focuses on enhancing the security and resilience of these memory systems.

A novel approach has been demonstrated with the implementation of a 2-bit Error Detection and Correction mechanism, integrating a Single Error Correction (SEC) decoder and a specialized debugging algorithm. This

dual-layer strategy represents a pioneering step towards fortifying the reliability and robustness of TCAM emulation techniques, marking a significant advancement in the field.

FUTURE SCOPE

Addressing double bit errors in TCAMS " is a field of research that deals with improving the reliability of ternary content-addressable memories (TCAMs) using error detection and correction techniques. TCAMs are widely used in network routers, firewalls, and other high- speed network devices for packet classification and routing.

Developing more efficient error detection and correction techniques: Researchers can explore new methods to detect and correct errors in SRAM emulated TCAMs that are more efficient than existing techniques. These techniques can reduce the overhead and improve the accuracy of error detection and correction.

Designing fault-tolerant SRAM emulated TCAM architectures: Researchers can focus on developing new architectures that are more fault-tolerant and can withstand more errors without compromising the accuracy of packet classification.

REFERENCES

- Autran, J. L., et al., "Soft-errors induced by terrestrial neutrons and natural alpha particle emitters in advanced memory circuits at ground level," Microelectron. Rel., vol. 50, no. 9, pp. 1822–1831, Sep. 2010.
- [2]. Bosshart, P., et al., "Forwarding metamorphosis: Fast programmable match-action processing in hardware for SDN," in Proc. ACM SIGCOMM, 2013, pp. 99–110.
- [3]. Chen, C. L., and Hsiao, M. Y., "Error-correcting codes for semiconductor memory applications: A stateof-the-art review," IBM J. Res. Develop., vol. 28, no. 2, pp. 124–134, Mar. 1984.
- [4]. Evans, A., Wen, S.-J., and Nicolaidis, M., "Case study of SEU effects in a network processor," in Proc. IEEE Workshop Silicon Errors Logic-Syst. Effects (SELSE), Mar. 2012, pp. 1–7.
- [5]. Fouzder, Tama, Abdul Hafeez Najib, ur Rehman, Omer Mujahid, "Power Efficient FPGA based TCAM Architecture by using Segmented Matchline Strategy", AECT conference, 2019.
- [6]. Kanekawa, N., Ibe, E. H., Suga, T., and Uematsu, Y., Dependability in Electronic Systems: Mitigation of Hardware Failures, Soft Errors, and Electro-Magnetic Disturbances, New York, NY, USA: Springer-Verlag, 2010.
- [7]. Pagiamtzis, K., and Sheikholeslami, A., "Content-addressable memory (CAM) circuits and architectures: A tutorial and survey," IEEE J. Solid-State Circuits, vol. 41, no. 3, pp. 712–727, Mar. 2006.
- [8]. Pontarelli, S., Ottavi, M., Evans, A., and Wen, S., "Error detection in ternary CAMs using Bloom filters," in Proc. Design, Automat. Test Eur. Conf. Exhib. (DATE), Mar. 2013, pp. 1474–1479.
- [10].Silburt, A. L., Evans, A., Perryman, I., Wen, S. J., and Alexandrescu, D., "Design for soft error resiliency in Internet core routers," IEEE Trans. Nucl. Sci., vol. 56, no. 6, pp. 3551–3555, Dec. 2009.

[9]. Reviriego, Pedro, Pontarelli, Salvatore, and Ullah, Anees, "Error Detection and Correction in SRAM Emulated TCAMs," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 2, Feb. 2019.